30 nm $In_{0.7}Ga_{0.3}As$ Inverted-Type HEMTs with Reduced Gate Leakage Current for Logic Applications

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Abstract

We have fabricated 30 nm $In_{0.7}Ga_{0.3}As$ Inverted-Type HEMTs with outstanding logic performance, scalability and high frequency characteristics. The motivation for this work is the demonstration of reduced gate leakage current in the Inverted HEMT structure. The fabricated devices show excellent L_g scalability down to 30 nm. L_g = 30 nm devices have been fabricated with exhibit g_m = 1.27 mS/μm, S = 83 mV/dec, DIBL = 118 mV/V, I_{ON}/I_{OFF} = 4 x 10^4, all at 0.5 V. More significantly, the removal of dopants from the barrier suppresses forward gate leakage current by over 100X when compared with equivalent normal HEMTs. The L_g = 30 nm devices also feature record high-frequency characteristics for an inverted-type HEMT design with f_T = 500 GHz and f_{max} = 550 GHz.

Introduction

As conventional Si CMOS scaling approaches the end of the roadmap, III-V based FETs appear as an increasingly viable alternative to continue transistor size scaling [1-2]. A great deal of the excitement about the prospects of III-Vs comes from the excellent logic characteristics that have recently been demonstrated in InGaAs HEMTs with gate lengths as small as 30 nm [3]. While being quite far in structure from an ideal logic III-V MOSFET, the HEMT has demonstrated to be an excellent model system to study fundamental device physics and technology issues and to provide well calibrated and relatively parasitic-free device results to support the development of simulators that would allows us to chart the future of a III-V logic technology [4].

In this regard, there is great value in continuing to push the scaling of HEMTs so as to explore significant device physics issues in the relevant dimensional range. It is well known that lateral scaling demands harmonious vertical scaling. Reduction of insulator thickness results in greatly increased gate leakage current [5]. This is what currently limits the reduction in HEMT lateral dimensions. Suppressing this, would allow us to scale the HEMT below 30 nm while preserving excellent logic characteristics. In this work, we demonstrated an inverted-type HEMT design that mitigates forward gate leakage current by over two orders of magnitude and yields excellent logic characteristics. This device architecture is also directly amenable to the incorporation of a high-K gate dielectric in the gate stack which should allow much further scaling.

Process Technology

Fig. 1 shows a cross section of epitaxial layer structure used in this work and a schematic of the fabricated device structure. Our device features an InAlAs/InGaAs double-heterostructure design where the upper Si-doping is located further away from the channel than in conventional designs (8 nm vs. about 3 nm). As a result, after a triple recess process [5], the dopant layer is eliminated in the intrinsic device resulting in a dopant-free InAlAs barrier. This gives rise to a conduction band shape for the barrier that, for the same sheet carrier concentration, is more rectangular than in the conventional design, as shown in **Fig. 2**. This should significantly suppress gate leakage current, especially in the forward gate bias regime.

Device fabrication follows closely our previous device demonstrations [6]. We use a three-step recess process that yields a barrier thickness in the intrinsic region, t_{ins}, of about 4 nm. In this work, we have devices with L_g values in the range of 30 to 130 nm. **Fig. 3** shows STEM images of a fabricated 30 nm device. The side-recess-length (L_{side}) was set at 80 nm.

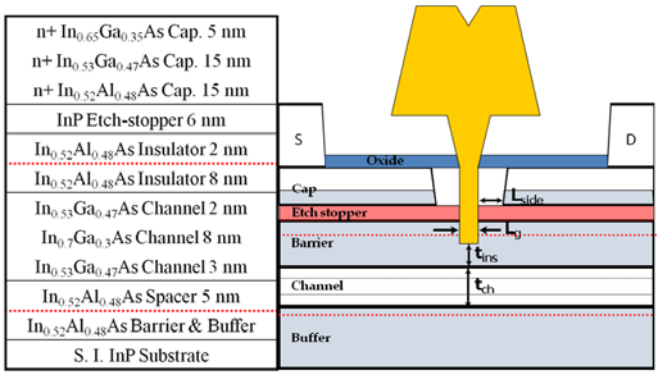

Fig. 1 Heterostructure and schematic of InGaAs Inverted HEMT. It features delta-doping in the top InAlAs layer that is etched away in the intrinsic device

DC and Logic Characteristics

Fig. 4 shows output characteristics of an inverted HEMT with L_g of 30 nm. The device exhibits excellent pinch-off and saturation characteristics. **Fig. 5** shows the subtreshold and gate current characteristics of a 30 nm I-HEMT against those of a previously demonstrated normal $In_{0.7}Ga_{0.3}As$ HEMT with a similar channel design, barrier thickness (4 nm), gate length, and L_{side} value. The inverted HEMT displays comparable subthreshold characteristics to the normal HEMT with a subthreshold swing of 83 mV/dec and DIBL of 118 mV/V at V_{DS} = 0.5 V. Remarkably, the inverted HEMT exhibits much lower values of OFF-state current and gate leakage current, especially in the forward regime where a reduction of over 100X is achieved.

Fig. 6 shows subthreshold characteristics for devices with L_g from 130 nm down to 30 nm at V_{DS} = 0.5 V, together with gate leakage current (I_G). The devices show harmonious scaling with very small V_T roll off in this dimensional range.

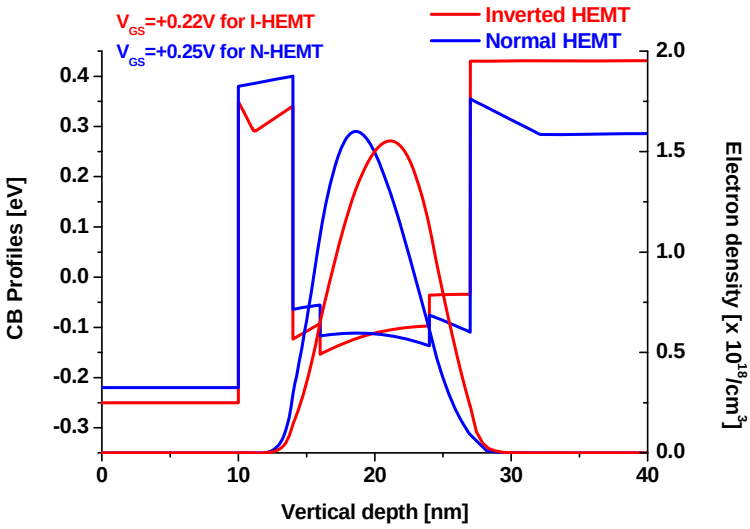

Fig. 2 Self-consistent Schrodinger-Poisson calculation of conduction band profile and electron density in Inverted HEMT and conventional HEMT at the same n_s = 1.3 x 10^{12}/cm^3.

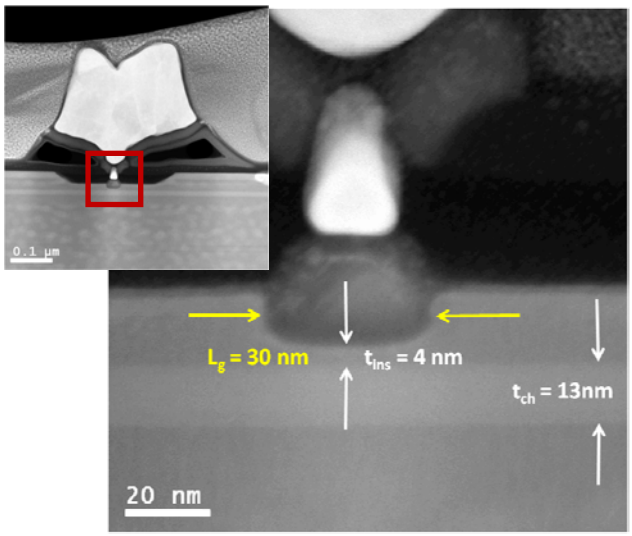

Fig. 3 Cross-section STEM images of inverted HEMT with L_G = 30 nm. The barrier thickness, t_{ins} is estimated to be 4 nm. [TEM analysis was carried out at NCNT and UNIST in Korea.]

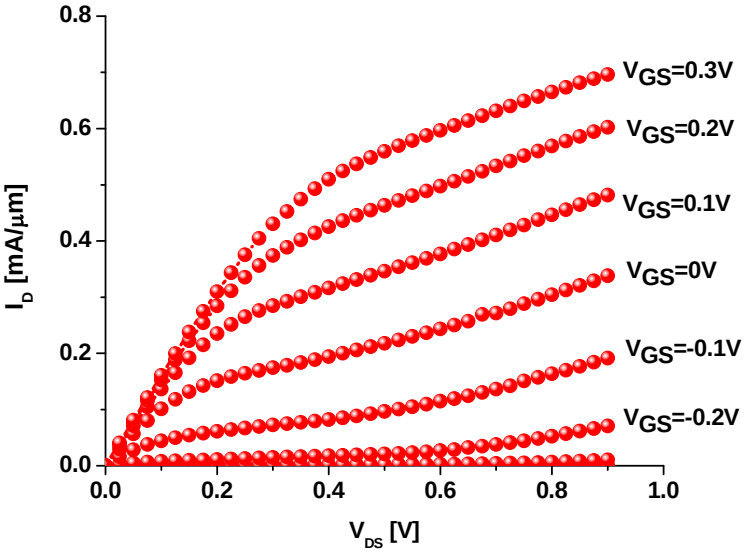

Fig. 4 Output characteristics of 30 nm InGaAs Inverted HEMT.

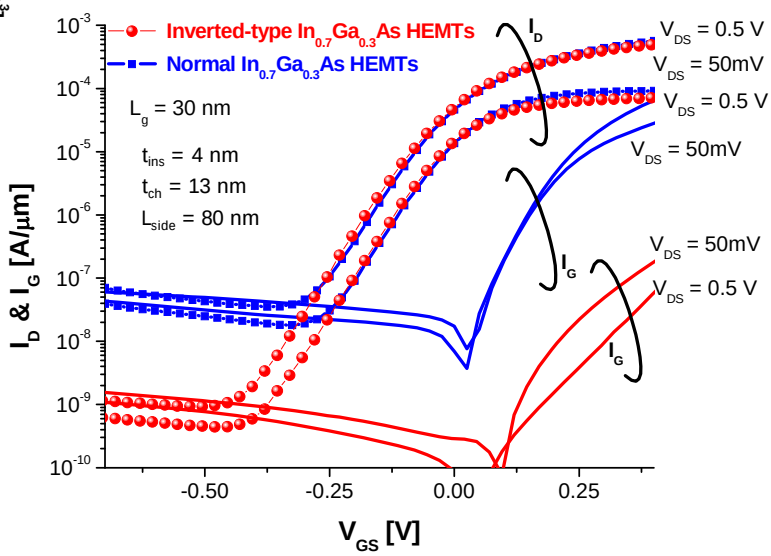

Fig. 5 Subthreshold and I_G characteristics of 30 nm InGaAs Inverted HEMT and normal HEMT. Off-state I_D and I_G characteristics are greatly suppressed in Inverted HEMT because of the rectangular shape of the barrier.

Fig. 7 shows I_{ON}, I_{OFF} and corresponding I_{ON}/I_{OFF} ratio as a function of L_g for both types of devices at V_{DS} = 0.5 V [7]. The inverted HEMT shows much lower values of I_{OFF}, and a significantly higher I_{ON}/I_{OFF} ratio across the entire dimensional rage when compared with the rectangular HEMT. At L_g=30 nm, the I_{ON}/I_{OFF} ratio is ~ 4 x 10^4. A trade-off of the inverted design is also evident in this figure. I_{ON} for the inverted HEMTs is slightly lower than for normal HEMTs. This comes from an increase in source resistance (R_s) which is a consequence of a reduction of the sheet carrier concentration in the extrinsic portion of the device as a result of having the upper Si-doping plane further away from the channel. This can be more quantitatively observed in **Fig. 8** which graphs the resistance measured though the gate-current

injection technique, R_s*, as a function of gate length [8]. The source resistance R_s can be extracted by linear extrapolation to zero Lg. The extracted R_s of I-HEMT is 0.27 Ω.mm, in contrast with 0.22 Ω.mm for the normal HEMT. Further improvement in I_{ON} can be obtained through optimization of the epitaxial design to achieve lower R_s.

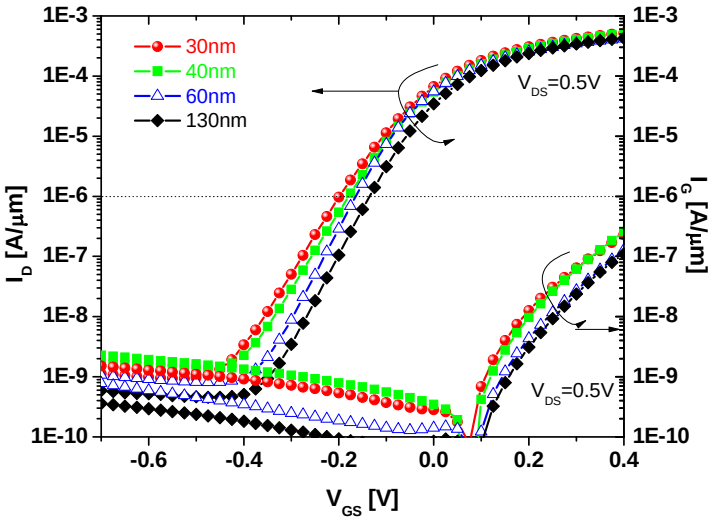

Fig. 6 Subthreshold and I_G characteristics for various values I-HEMTs with different values of L_g at V_{DS} = 0.5 V. There is a slight negative shift of V_T as L_g scales down to 30 nm.

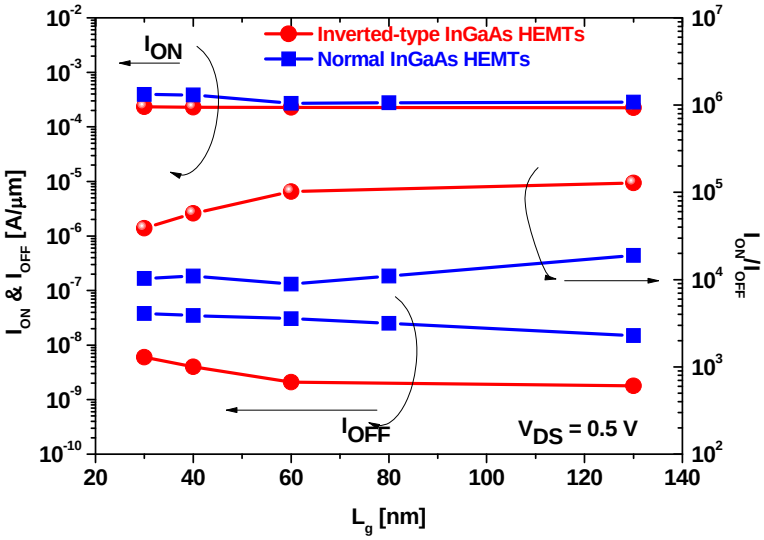

Fig. 7 I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio vs. L_g for both InGaAs HEMTs. The Inverted HEMT shows significantly improved I_{ON}/I_{OFF} ratio at all gate lengths.

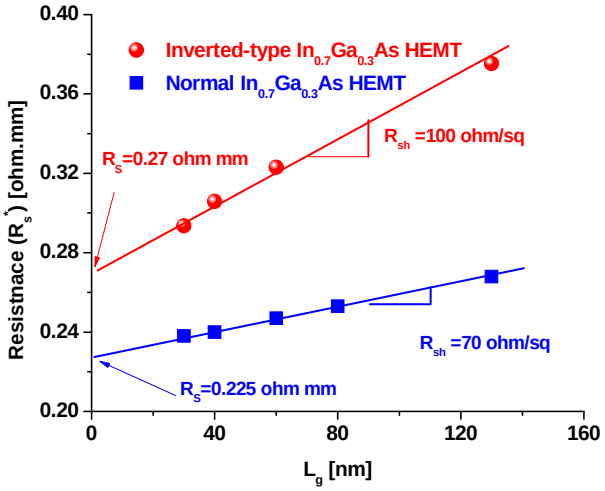

Fig. 8 Measured R_s* as a function of L_g through the gate current injection technique. Inverted HEMT shows a higher source resistance and sheet resistance of the channel under the gate.

Microwave and Logic Performance

Microwave performance was characterized from 0.5 to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductances from the measured device S-parameters. **Fig. 9** plots the f_T and f_{max} as a function of V_{GS} at V_{DS} = 0.8 V for L_g=30 nm Inverted and normal HEMTs. Excellent values of f_T = 500 GHz and f_{max} = 550 GHz have been obtained for the I-HEMT. These are the highest values of f_T and f_{max} ever reported in an Inverted HEMT. f_T is lower than in the normal HEMT but f_{max} is significantly higher. This is due to improved output conductance (g_o) characteristics. In order to understand the somehow reduced f_T of the inverted HEMT, **Fig. 10** shows extrinsic ($g_{m,ext}$) and intrinsic peak transconductance (g_{mi}) which is extracted from S-parameters after removal of source and drain resistance. g_{mi} for the Inverted HEMT is lower than that of normal HEMT. This comes from somehow poorer transport in the channel which also manifests itself through a lower electron mobility in the epitaxial structure (μ_e ~ 9,800 vs. 11,000 $cm^2/V.s$ in the normal HEMT). This is a known drawback of the inverted HEMT design with arises from increased interface roughness of the reverse InGaAs/InAlAs interface [9]. Improved epitaxial growth techniques should mitigate this problem.

To identify the significance of the results obtained in this work, we have benchmarked the logic performance of our devices against advanced Si CMOS technologies. **Fig. 11** summarizes the subthreshold swing against L_g for our inverted HEMT together with normal HEMTs, as well as advanced Si CMOS. Excellent electrostatic integrity is evident. A similar result is obtained for DIBL. We have also performed a rigorous comparison of the logic performance of our inverted and normal HEMTs with L_g = 30 nm and state-of-the-art 65 nm Si CMOS which has a similar gate length [3, 5]. **Fig. 12** plots I_{ON} against I_{leak} characteristics at 0.5 V. I_{leak}

takes into account the forward gate leakage current and it is a more appropriate figure of merit for devices that suffer from significant gate leakage [5]. We find that at an I_{leak} of 100 nA/μm, 30 nm Inverted HEMT exhibit 29% higher current drive (I_{ON}) than 65 nm High Performance (HP) CMOS technology with L_g = 35 nm and 20 % higher current drive (I_{ON}) than normal HEMT with L_g = 30 nm.

Conclusions

We have demonstrated 30 nm $In_{0.7}Ga_{0.3}As$ Inverted HEMTs with outstanding logic performance, scalability and high frequency characteristics. In particular, 30 nm devices exhibit $g_{m,max}$ = 1.27 mS/μm, S = 83 mV/dec, DIBL = 118 mV/V, $I_{ON}/I_{OFF} = 4 \times 10^4$, at V_{DS} = 0.5 V, and f_T = 500 and f_{max} = 550 GHz at V_{DS} = 0.8 V. The removal of dopants from the barrier suppresses forward gate leakage current by over 100X. This works suggest that III-V designs similar to an inverted HEMT but with a high-K dielectric as gate insulator have potential for scaling to very small dimensions.

References

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Acknowledgements

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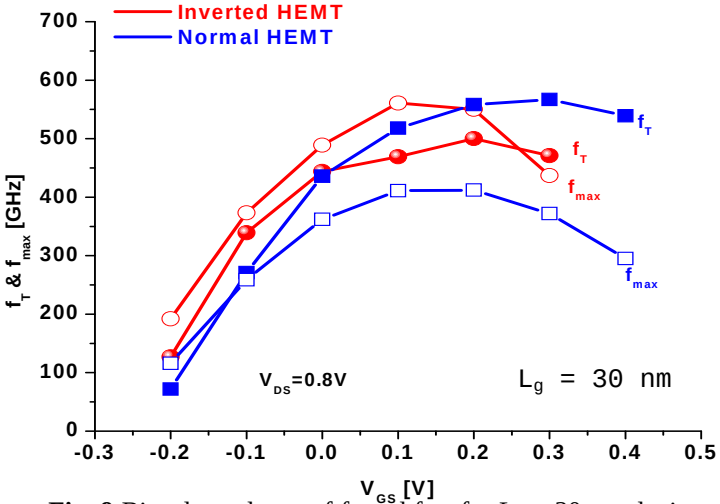

Fig. 9 Bias dependence of f_T and f_{max} for L_g = 30 nm devices at V_{DS} = 0.8 V.

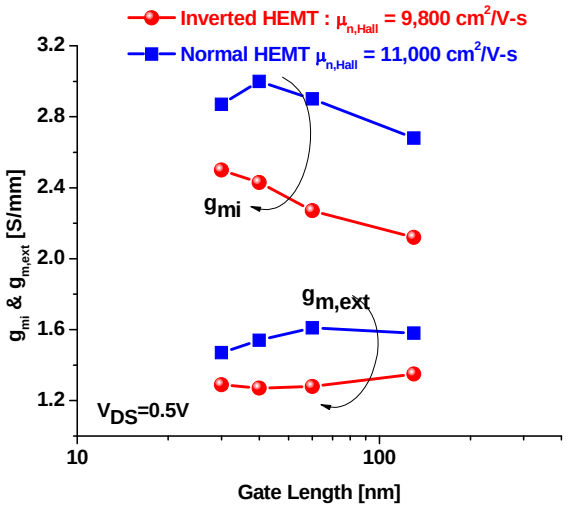

Fig. 10 Intrinsic transconductance (g_{mi}) and extrinsic transconductance ($g_{m,ext}$) as a function of gate length.

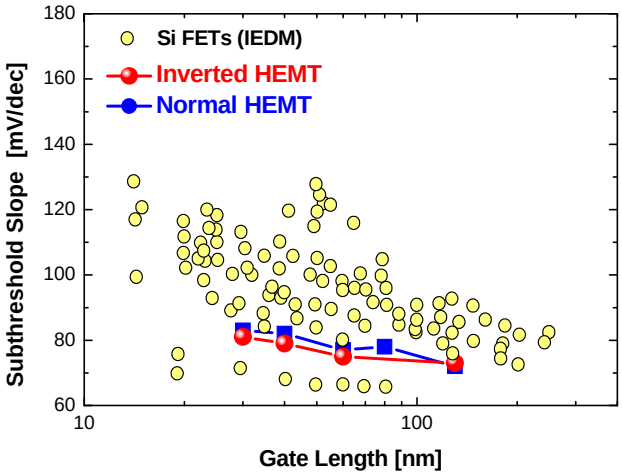

Fig. 11 Subthreshold swing of Inverted and Normal InGaAs HEMTs as a function of L_g, together with those of advanced Si nFETs.

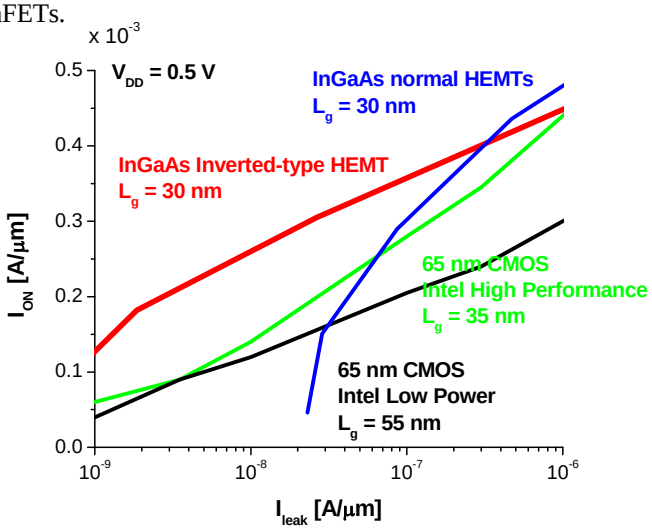

Fig. 12 I_{ON} against I_{leak} for 30 nm InGaAs HEMTs, and both low-power and high-performance 65 nm CMOS, all at V_{DD} = 0.5 V.